PATENT ABSTRACTS OF JAPAN

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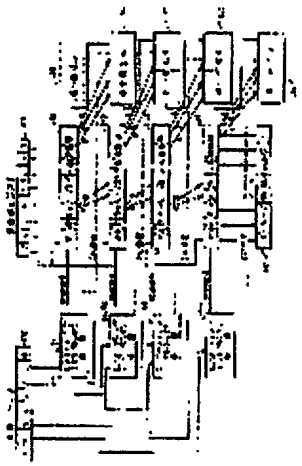
(54) DEVICE AND METHOD FOR QUICKENING INTEGER AND FLOWING-POINT MULTIPLICATION

(57)Abstract:
PURPOSE: To quicken multiplying operation by generating plus logic signals by plural encoding means in response to a previously selected multiplication operand signal and sending them to a 1st carry/save adding means at a previously set digit.
CONSTITUTION: A multiplication unit consisting of plural carry/save adder stages 111-114 is provided and its multiplication procedure is followed by using correction booth algorithm. For example, when encoded multiplier bits representing subtracting operation are needed, subtracting operations is all performed by adding operation. Therefore, a single signal of logic '1' needed to convert a group of signals of a complement of 1 derived from the multiplication operand into a group of signals of a complement of 2 is inputted to the 1st carry/save adder stage 111 at a proper bit position. Consequently, the multiplication can be quickened.



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